After Final Office Action of May 13, 2008

REMARKS

Docket No.: M4065.0087/P087-A

Applicant thanks the Examiner for the courtesy of the interview on September 9, 2008, wherein an agreement was reached as to the patentability of the claims, as amended herein, over the cited references. Applicant gratefully acknowledges the acceptance of the drawings filed on September 15, 2003, the consideration of all references cited in the IDS filed September 14, 2003, the withdrawal of objections to claims 80 and 84 made in the Office Action dated October 26, 2007, and the withdrawal of the obviousness-type double patenting rejection of claims 80, 81, 83-89, and 91 in the same Office Action. Claims 80, 82-84, 86-88, 93, 97, 99, 101, 102, and 106 are amended. Claims 1-79 were previously cancelled, without prejudice. A Request for Continued Examination is filed herewith. Applicant also respectfully petitions for a one (1) month extension of time and submits the requisite fee herewith.

Claims 80-83, 88-96, 102-104, and 106 stand rejected under 35 U.S.C. § 102(b) as anticipated by U.S. Patent 5,721,422 ("Bird"). Applicant respectfully traverses this rejection.

Claim 80 defines a method of operating an active pixel CMOS imager and recites "activating a first pixel in a row of pixels connected to a shared column line using a first row select line and then subsequently activating an adjacent second pixel in the row of pixels connected to the shared column line using a second select row line, wherein the first row select line and the second row select line each run along the row of pixels and are not connected to pixels of any other row of the array, the first and second pixels disposed in a pixel array; resetting a voltage level of a node to a predetermined voltage using a reset transistor addressed by a reset line that extends approximately linearly across the pixel array; transferring charge collected by the first pixel to the node; detecting the charge at the node; and generating an output signal over the shared column line corresponding to the charge detected at the node." No such method is disclosed by Bird.

Bird fails to disclose "activating a first pixel in a row of pixels connected to a shared column line using a first row select line and then subsequently activating an adjacent second pixel in the row of pixels connected to the shared column line using a second select row line, wherein the first row select line and the second row select line each run along the row of pixels and are not

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connected to pixels of any other row of the array, the first and second pixels disposed in a pixel array" as recited by claim 80. For at least this reason, independent claim 80 is not anticipated by Bird. Therefore, claims 81-83 that depend from claim 80 are also not anticipated by Bird. Applicant respectfully requests that the 35 U.S.C. § 102(b) rejection of these claims be withdrawn and the claims allowed.

Claim 88 defines an active pixel CMOS imager and recites "a plurality of pixels to generate an output signal associated with detected light, the plurality of pixels arranged in rows and columns of an array, each said row having both odd and even pixels; a plurality of column lines each connected to at least two adjacent pixels of a row in the array, the column lines being connected to output circuitry to output the signal; a plurality of odd row select lines orthogonal to the column lines to address odd pixels in the rows; a plurality of even row select lines orthogonal to the column lines to address even pixels in the rows, wherein the even row select lines do not address the odd pixels and the odd row select lines do not address the even pixels; a column driver to address pixels connected to the column lines; and a row driver to address pixels through the odd row select lines and the even row select lines." Bird does not disclose such a device.

Bird fails to disclose "a plurality of pixels to generate an output signal associated with detected light, the plurality of pixels arranged in rows and columns of an array, each said row having both odd and even pixels" and "a plurality of odd row select lines orthogonal to the column lines to address odd pixels in the rows; a plurality of even row select lines orthogonal to the column lines to address even pixels in the rows, wherein the even row select lines do not address the odd pixels and the odd row select lines do not address the even pixels," as recited by independent claim 88. For at least this reason, independent claim 88 is not anticipated by Bird. Therefore, claims 89-92 that depend from claim 88 are also not anticipated by Bird. Applicant respectfully requests that the 35 U.S.C. § 102(b) rejection of these claims be withdrawn and the claims allowed.

Claim 93 defines a method of operating a CMOS imager and recites "addressing even pixels in a row of pixels of an array of pixels using a row driver coupled to an even row select line; providing a first output signal associated with light detected by the even pixels to a plurality of column lines coupled to the even pixels; addressing odd pixels in the row of pixels via an odd row

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select line, wherein the even row select lines do not address the odd pixels and the odd row select lines do not address the even pixels; and providing a second output signal associated with light detected by the odd pixels to the plurality of column lines coupled to the odd pixels." Such a method is not disclosed by Bird.

Bird fails to disclose "addressing odd pixels in the row of pixels via an odd row select line, wherein the even row select lines do not address the odd pixels and the odd row select lines do not address the even pixels," as recited by independent claim 93. For at least this reason, independent claim 93 is not anticipated by Bird. Therefore, claims 94-96 that depend from claim 93 are also not anticipated by Bird. Applicant respectfully requests that the 35 U.S.C. § 102(b) rejection of these claims be withdrawn and the claims allowed.

Claim 102 defines an imaging device and recites "a pixel array comprising a row comprising a plurality of first pixels and a plurality of second pixels; a first row address line connected with the first pixels; a second row address line connected with the second pixels, wherein the second row address line is not connected with the first pixels and the first row address line is not connected with the second pixels; a respective column line for each pair of first and second pixels of the row; and a reset line connected to the plurality of first pixels." This device is not disclosed by Bird.

Bird fails to disclose "a pixel array comprising a row comprising a plurality of first pixels and a plurality of second pixels; a first row address line connected with the first pixels; a second row address line connected with the second pixels, wherein the second row address line is not connected with the first pixels and the first row address line is not connected with the second pixels; a respective column line for each pair of first and second pixels of the row," as recited by independent claim 102. For at least this reason, independent claim 102 is not anticipated by Bird. Therefore, claims 103-105 that depend from claim 102 are also not anticipated by Bird. Applicant respectfully requests that the 35 U.S.C. § 102(b) rejection of these claims be withdrawn and the claims allowed.

Claim 106 defines an imaging device and recites "a row of pixels comprising a first plurality of pixels and a second plurality of pixels, a first address line addressing only the first plurality of said pixels and a second address line addressing only the second plurality of said pixels; a plurality of read-out lines, each of said read-out lines being connected to a first pixel of the first plurality of pixels and a second pixel of the second plurality of pixels; and a reset line connected to at least the first plurality of pixels or the second plurality of pixels." Such a device is not disclosed by Bird.

Bird fails to disclose "a row of pixels comprising a first plurality of pixels and a second plurality of pixels, a first address line addressing only the first plurality of said pixels and a second address line addressing only the second plurality of said pixels," as recited by independent claim 106. For at least this reason, independent claim 106 is not anticipated by Bird. Applicant respectfully requests that the 35 U.S.C. § 102(b) rejection of this claim be withdrawn and the claim allowed.

Claims 84-87 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Bird in view of U.S. Patent 5,576,763 ("Ackland et al."). Applicant respectfully traverses this rejection.

Claim 84 defines a method of operating a system and recites "focusing an image on an active pixel CMOS imager, the imager comprising a pixel array; activating a first pixel in a row connected to a shared column line using a first row select line and then subsequently activating an adjacent second pixel in the row connected to the shared column line using a second row select line, the pixel array comprising the first and second pixels and the first row select line and second row select line each running along the length of the row and not being connected to pixels of any other row; resetting a voltage level of a node associated with the first pixel to a predetermined voltage using a reset transistor addressed by a reset line that extends approximately linearly across the pixel array; transferring charge collected by the first pixel to the node; detecting the charge at the node; and generating an output signal over the shared column line, the output signal corresponding to the image." This method is not taught or suggested by the combination of Bird and Ackland et al.

The combination of Bird and Ackland et al. fail to disclose, teach, or suggest "activating a first pixel in a row connected to a shared column line using a first row select line and then subsequently activating an adjacent second pixel in the row connected to the shared column line using a second row select line, the pixel array comprising the first and second pixels and the first row select line and second row select line each running along the length of the row and not being connected to pixels of any other row," as recited by independent claim 84. For at least this reason, independent claim 84 is patentable over the combination of Bird and Ackland et al. Therefore, claims 85-87 that depend from claim 84 are also patentable over the combination of Bird and Ackland et al. Applicant respectfully requests that the 35 U.S.C. § 103(a) rejection of these claims be withdrawn and the claims allowed.

Claims 97-101 and 105 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Bird in view of U.S. Patent 5,587,738 ("Shinohara"). Applicant respectfully traverses this rejection.

Claim 97 defines an imaging device and recites "a row comprising a first pixel and a second pixel; the first and second pixels being joined by a diagonal active area component; a first even row line connected with the first pixel; a second odd row line connected with the second pixel, wherein said first even row line and said second odd row line are associated with said row and not any other row; and a column line connected with the first and second pixels at the diagonal active area component." Such a device is not taught or suggested by the combination of Bird and Shinohara.

Bird and Shinohara, combined, fail to disclose, teach, or suggest "a first even row line connected with the first pixel; a second odd row line connected with the second pixel, wherein said first even row line and said second odd row line are associated with said row and not any other row," as recited by independent claim 97. For at least this reason, independent claim 97 is patentable over the combination of Bird and Shinohara. Therefore, claims 98-101 that depend from claim 97 are also patentable over the combination of Bird and Shinohara. Applicant respectfully requests that the 35 U.S.C. § 103(a) rejection of these claims be withdrawn and the claims allowed.

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Claim 105 depends from claim 102, which recites "a pixel array comprising a row comprising a plurality of first pixels and a plurality of second pixels; a first row address line connected with the first pixels; a second row address line connected with the second pixels, wherein the second row address line is not connected with the first pixels and the first row address line is not connected with the second pixels; a respective column line for each pair of first and second pixels of the row," and is incorporated into claim 105. The combination of Bird and Shinohara fails to disclose, teach, or suggest such a combination of features. For at least this reason, claim 105 is patentable over the combination of Bird and Shinohara. Applicant respectfully requests that the 35 U.S.C. § 103(a) rejection of this claim be withdrawn and the claim allowed.

In view of the above, Applicant believes the pending application is in condition for allowance. A notice of allowance is respectfully solicited.

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Respectfully submitted,

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